Amendments to the Specification:

Please amend paragraphs [27], [28], and [30] of the specification as follows. This amendment adds no new matter to the patent application.

[27] **FIG. 5** is block diagram of a synchronous servo circuit ***60***, which in accordance with an embodiment of the invention includes a synchronization-mark-and-polarity detector ***62*** for recovering a synchronization mark such as the sync mark of Table I below, determining the connection polarity of a read-write head (**FIG. 9**) from the recovered sync mark, and causing a phase-compensation circuit ***64*** to adjust the phase of the servo signal if the head connection is reversed. The detector ***62*** is further discussed below in conjunction with **FIG. 6**, and in one embodiment, the detector ***62*** includes a polarity-independent first Viterbi detector ***100*** and the circuit ***64*** includes a conventional twos-compliment inverter.

[28] The circuit ***60*** also includes a gain and filter circuit ***66***, which adjusts the gain of, filters, and equalizes the servo signal from the read-write head (**FIG. 9**). An analog-to-digital converter (ADC) ***68*** receives a sample clock (not shown) on a control bus ***70*** and generates digital samples of the servo signal from the circuit ***66***. A finite-impulse-response (FIR) filter ***72*** boosts the equalization of the samples received from the ADC ***68*** via the phase-compensation circuit ***64***, and timing and gain recovery loops ***74*** effectively synchronize the sample clock to the servo signal and maintain the gain of the circuit ***60*** at a desired level. The phase-compensation circuit ***64***, ADC ***68***, FIR ***72***, and loops ***74*** form a sample circuit ***76***. A second Viterbi detector ***78*** recovers servo data, such as the location identifier ***38*** (**FIG. 3**), from the servo-signal samples generated by the loops ***74***. A decoder ***80*** decodes the recovered servo data from the Viterbi detector ***78*** in response to a Sync Mark Detect signal from the detector ***62***. A position-burst demodulator ***82*** receives samples of the servo signal from the FIR ***72*** and generates a head-position-error signal, and a processor ***84*** controls the components of the servo circuit ***60*** via the control bus ***70***. For example, the processor ***84*** causes the circuit ***64*** to invert the samples from the ADC ***68*** in response to a predetermined logic level of a Head Polarity signal from the detector ***62***. A servo-data interface ***86***

interfaces the decoder ***80***, demodulator ***82***, and processor ***84*** to a disk-drive controller (**FIG. 9**). Alternatively, as discussed below, depending on the scheme used to code the servo data, the circuit ***60*** may omit the second Viterbi detector ***78*** and use the detector ***62*** to recover all of the servo data. Furthermore, although shown located between the ADC ***68*** and the FIR ***72***, the phase-compensation circuit ***64*** may be located elsewhere in the forward path of the servo circuit ***60*** such as at the input of the Viterbi detector ***78***.

[30] **FIG. 6** is a block diagram of the synchronization-mark-and-polarity detector ***62*** of **FIG. 5** according to an embodiment of the invention. The detector ***62*** includes [[a]] the polarity-independent first Viterbi detector ***100***, which recovers the sync mark from the servo signal regardless of the head-connection polarity and which includes a bank ***102*** of path-history registers PH00 – PHZ, one register for each state that the Viterbi detector ***100*** recognizes. A comparator ***104*** detects the sync mark and the head-connection polarity by comparing the recovered servo data from the Viterbi detector ***100*** with the noninverted version of the sync mark stored in a register ***106***. The comparator ***104*** generates the Sync Mark Detect signal having one logic level when it detects the sync mark and another logic level otherwise, and generates the Head Polarity signal having one logic level when the head is properly connected to the servo circuit ***60*** (**FIG. 5**) and another logic level when the head connection is inverted. Alternatively, where the second Viterbi detector ***78*** (**FIG. 5**) is omitted, the servo circuit ***60*** (**FIG. 5**) uses the first Viterbi detector ***100*** to recover all of the servo data and to provide the recovered servo data to the decoder ***80***.